Prof. Chandankar (Lec. 11)
Dt : 28/3/12

LOGIC REPRESENTION OF ADDER

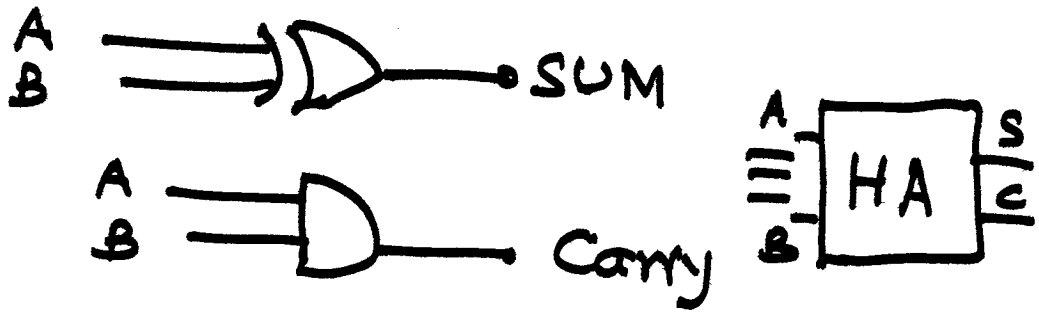
2 Bit Adder

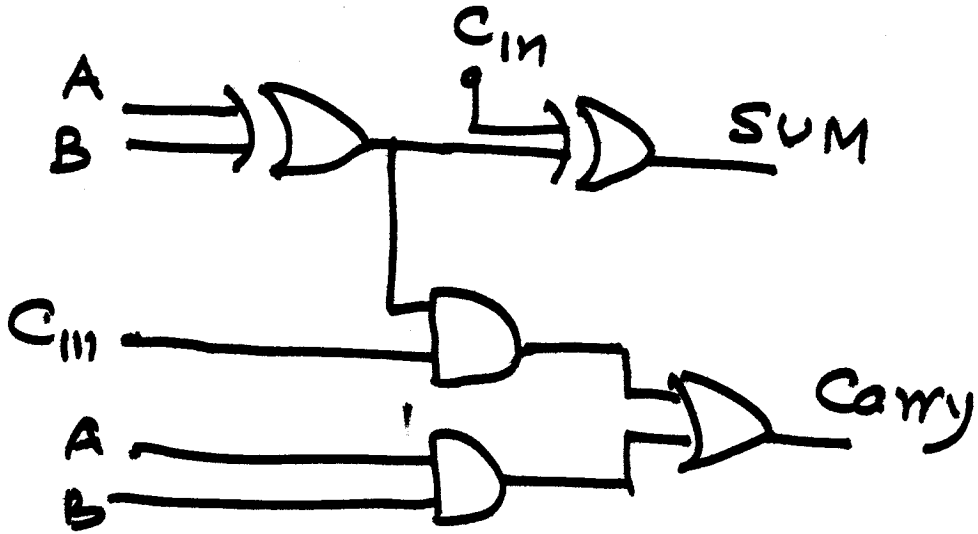
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

With Initial Carry C_{in}

$$S = A \oplus B \oplus C_{in}$$

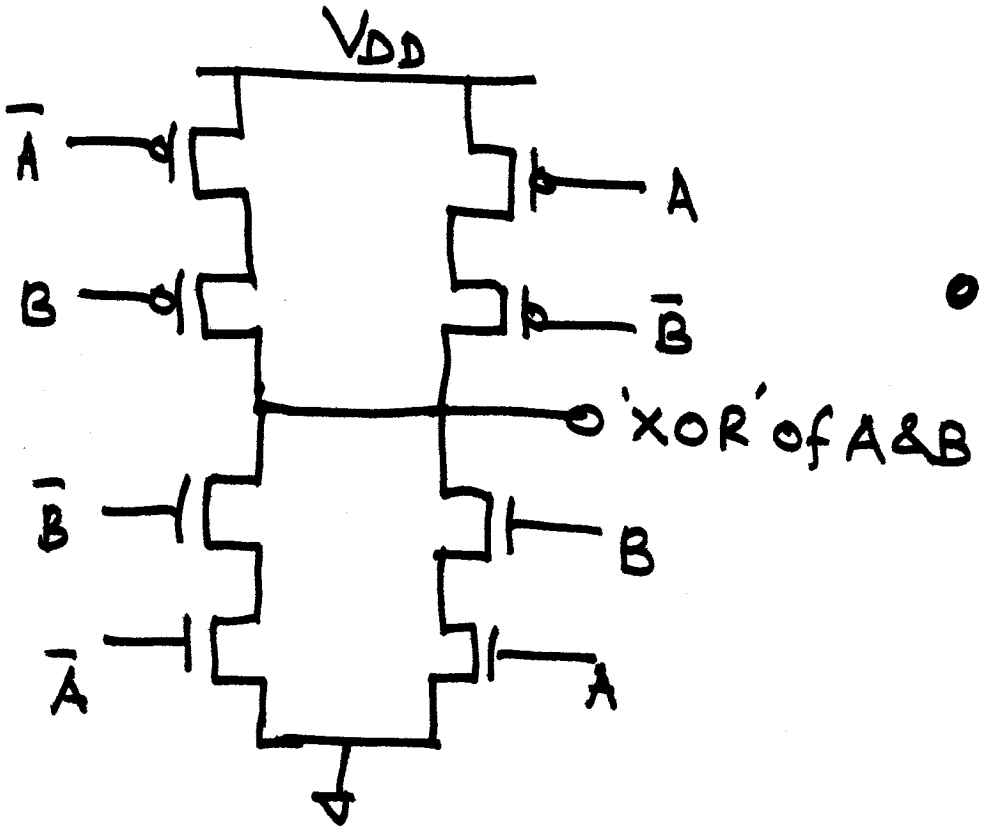
$$C_{out} = (A \oplus B).C_{in} + A.B$$





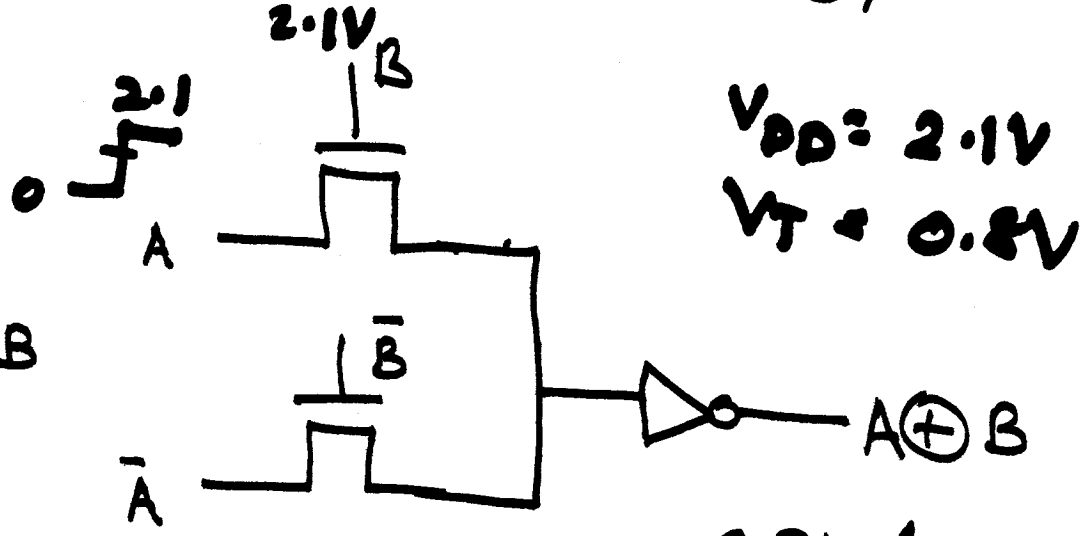
Full Adder

DESIGN STYLE FOR 'XOR' IN CMOS Technology



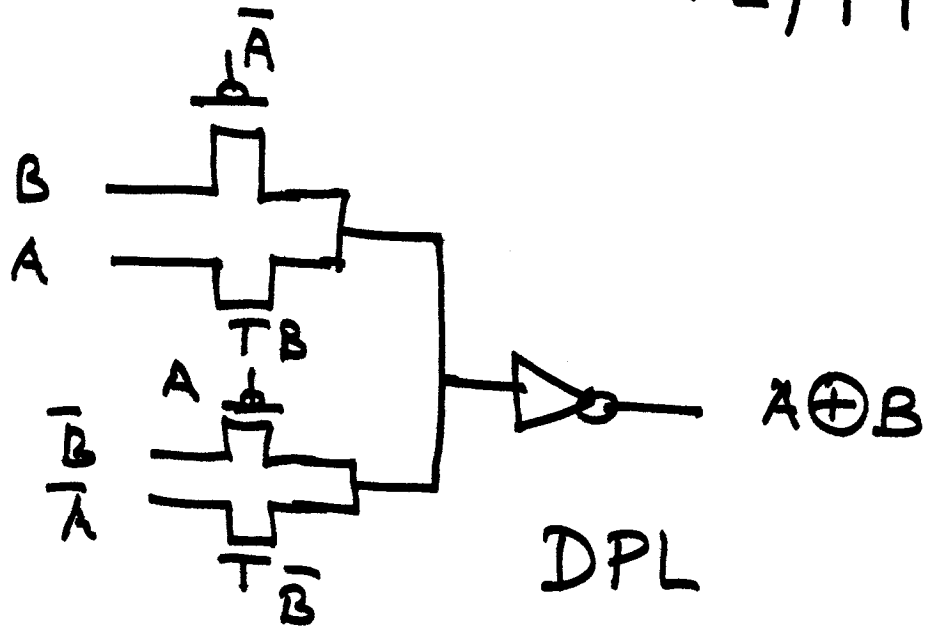
Static CMOS

$$A \oplus B = \overline{(AB + \bar{A}\bar{B})}$$



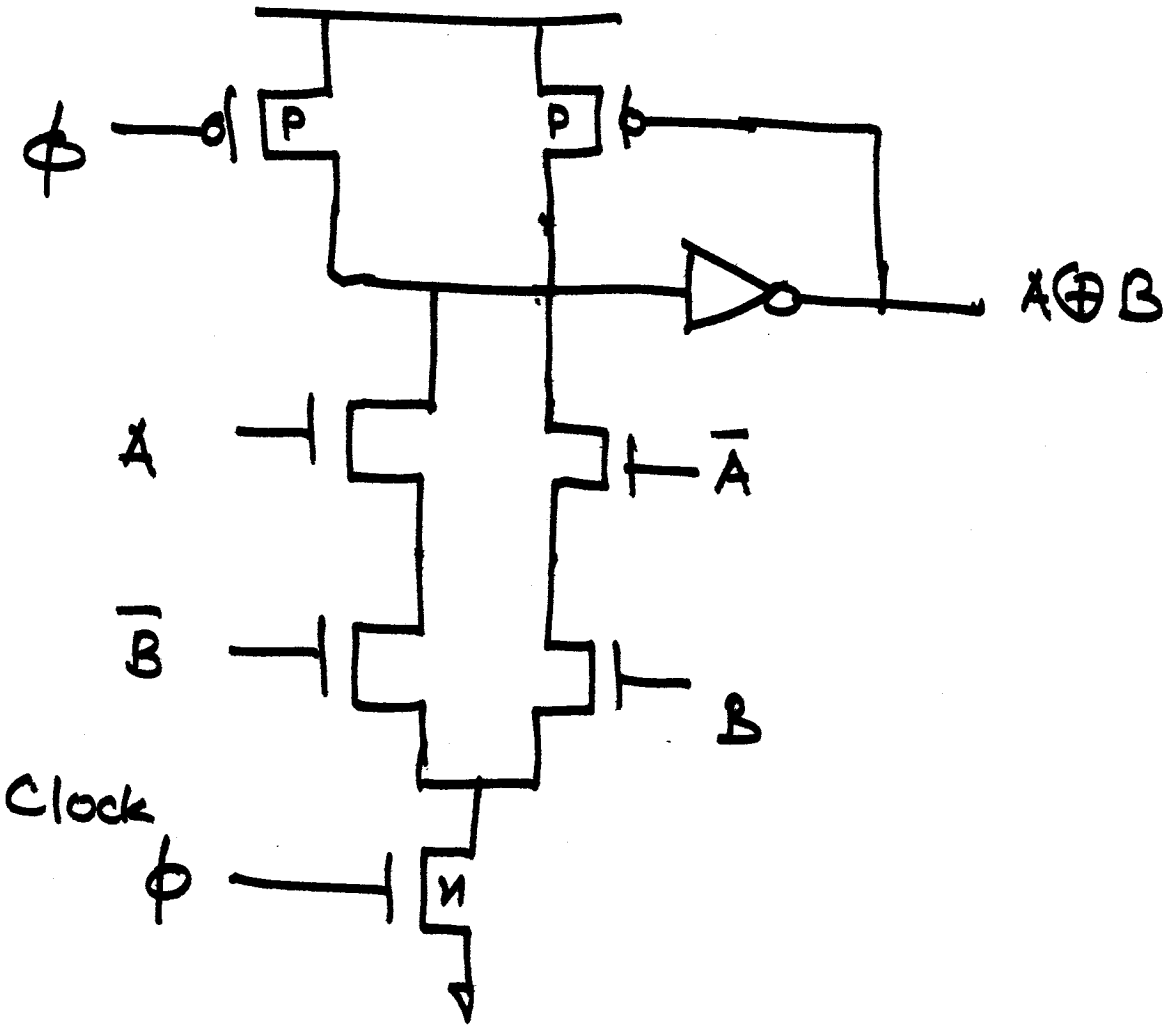
V_{DD} = 2.1V
V_T = 0.8V

CPL / PTL



DPL

DUAL RAIL DOMINO



COMPARISION OF DESIGN STYLES FOR ADDER CIRCUIT

Parameter	Static CMOS	CPL	DPL	Dual Rail DOMINO
Power(mW)	34.3	34.5	27.5	82.5
Worst Case Delay (ns)	2.33	2.24	1.98	1.78
Energy (μJ)	79.9	77.3	54.5	146.9
Area: in Total Transistor Width (μm)	27355	17437	19117	32444

Σ. Technology : $V_{DD} = 3.3V$, $f = 100MHz$